Electrical Characterization and Reliability Test on TSV Structure for 3D Stack Packaging

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ABSTRACT

To assess the reliability behavior of a typical TSV structure, this study performed reliability tests on self-design samples with three types of the TSV test-keys, which includes the Kelvin structure, the via-chain structure, and the meander metal lines. With enough number of the samples for statistic analyses, resistance of the test samples were first found increased after the preconditioning process. The reliability tests were next carried out according to the JEDEC standards, and the Weibull parameters for the testing samples were then extracted from the testing data to predict the lifetime performance on the samples. Finally, OM and SEM observations on the test samples are given for failure analyses.

Keywords: TSV (Through Silicon Via), Reliability, Temperature Cycling Test (TCT), Temperature Humidity Cycling Test (THCT)

TSV 結構三維堆疊構裝技術之電性可靠度分析

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摘　　要

直通矽晶穿孔技術能提供上下垂直導通之路徑，成為具有三維堆疊構裝技術之潛力。為了解直通矽晶穿孔三維堆疊構裝技術之可靠度問題，本研究開發製作 Kelvin 結構、鏈狀式結構路徑總電阻及金屬導線電阻等三種測試鍵，並依據 JEDEC 規範針對三種測試鍵執行溫度循環測試及熱濕循環測試分析，從中量測 TSV 堆疊架構產品之生命週期，進一步分析可靠度模型及萃取韋伯參數。最後，使用光學顯微鏡與掃描式電子顯微鏡觀察測試元件損害分析，提供直通矽晶穿孔技術可靠度分析參考依據。

關鍵詞：直通矽晶穿孔技術，可靠度，溫度循環測試，熱濕循環測試

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I. INTRODUCTION

As the semiconductor technology development trend is towards higher density, size reduction on the conventional two-dimensional (2D) electronic packaging becomes a must so that the three-dimensional (3D) stacking packaging was developed. Consequently, the 3D packaging integration with through silicon via (TSV) technology becomes one of the mainstreams of the packaging industry in recent years because it takes the advantages of higher density, higher performance, lower power consumption, lower parasitic effects, and possibly lower cost for heterogeneous integration. As a result, the TSV technology was first applied on memory chips, RF devices, and CMOS image sensors (CIS), and its applications are gradually expanding to ASIC and MEMS according to the Yole's report [1].

Researches on electrical characterization, process yield evaluations, and device reliability of the TSV structures are available in the literature. To understand the life time and the failure mode of a chips stacking structure with silicon through vias, Kuo et al. performed pre-condition test, temperature cycling test (TCT), and pressure cooker test (PCT) to qualify the samples [2], and Seung, et al. constructed the temperature cycle solder joint reliability test to discuss the environmental factor on signal interconnections among the layers [3]. To verify the performance, yield, and reliability of the TSV structure, Trigg,et al. designed their test chip which is suitable for the tests on thermal, stress, electromigration, and moisture effect [4]. In addition, Cassidy et al. discussed the reliability assessments such as residual stress, resistance, leakage, and dielectric breakdown [5]; Frank et al. analyzed TSV interconnects from high density Cu TSV-last and Cu TSV-middle process to study reliability on electromigration and thermal cycling, and examined the impacts on metal level dielectric [6], and Okoro et al. provided the radio frequency based measurement technique as a metrology tool to assess thermal cycling effect on stacked TSV-die reliability [7]. However, the aforementioned tasks were either oversimplified or short of testing samples for statistic analyses. To this end, a complete reliability study on typical TSV structures was proposed and performed in this paper based on our earlier experiences on TSV property analyses with several self-design test patterns [8].

Since the electrical performances on the interconnections and the vias are the key factors on TSV reliability, adequate test patterns were proposed and manufactured in this study through the via-last process on 8-inch wafers which is applied to the CMOS image sensor (CIS) packaging with 3D Wafer Level Packaging (3D-WLP) technology. For better statistical meaning, more than 50 samples cut from different test wafer location were prepared for each type of the test patterns. After the first measurements on the qualified test patterns to obtain the initial performances of the samples, preconditioning with baking and moisture soaking were executed and the results were analyzed. Experiments on testing sample reliabilities were next carried out with temperature cycling test (TCT) and temperature humidity cycling test (THCT) according to the JEDEC (Joint Electron Device Engineering Council) standards. Finally, the Weibull distribution model was employed for the reliability analyses to extract the Weibull parameters for the test patterns, and the failure analyses were reported. It is concluded that the extracted parameters are useful for the reliability and the lifetime performance analyses on the TSV structures.

II. THE EXPERIMENTAL PROCEDURES

In this study, The via-last TSV test patterns were first made on 8-inch wafers through a commercialized 1P3M (one poly-silicon layer and three metal layers) CMOS process with 0.18 μm technology, and the wafers were next bonded with a glass carrier wafer for wafer thinning until 120 μm of thickness. Packaging processes such as silicon etching, CVD isolation, oxide etching, PVD seeding, metal redistribution, passivation, and ball mounting were then performed afterward. Note that all of the aforementioned processes were constrained in low temperature conditions (less than 200°C within 1 hour and less than 260°C in a few minutes). The three test patterns on the test samples include:

(1) The meander metal lines on the copper redistribution layer (RDL) for the sheet resistance (R_{sh}) measurements through the

four-point probe (4PP) tests. The width and length of the metal lines are 30μm and 4470μm, respectively, and the line spacing is 30μm.

(2) The daisy-chain or the via-chain of the TSV structures, as shows in Figure 1, with 15 vias for the total resistance (R_t) measurements to illustrate electrical continuity and/or the leakage conditions on the samples. Measurements through the two-point probe (2PP) tests were performed on the via-chain samples.

(3) The Kelvin structure as shows in Figure 2 to measure the contact resistance (R_c) between the copper redistribution layer trace (Metal 2) and the aluminum conducting lines (Metal 1) at the via bottom through the 4PP tests. Note that the contact resistance is the key parameter to address the electrical performance of a TSV, and it is affected by many design and process parameters such as the opening area at the TSV bottom, the barrier layer thickness, and the seed layer type.

In this work, electrical behaviors on the testing samples were measured by an Agilent 4156C Precision Semiconductor Parameter Analyzer, and each of the resistance were obtained by linear fitting from 100 measured I-V points. For better statistic meaning, totally 104 samples for the R_t and R_c tests and 52 samples for the R_{sh} tests were prepared, respectively. Details of the test results are discussed in the next sections.

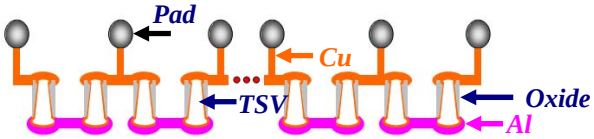

Fig. 1. The via chain structure.

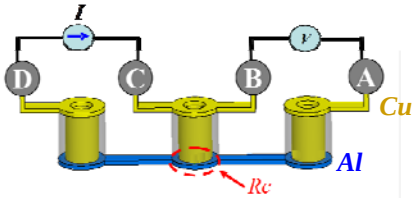

Fig. 2. The Kelvin structure with the 4PB measurement.

III. THE PRECONDITIONING

Prior to the reliability tests, preconditioning was performed to simulate the effects due to board assembly. To this end, we first measured the initial value of the contact resistance (R_c) and total resistance (R_t), and divided the chips into groups (Center, Left, Right, Up, and Down) according to their locations from the test wafers. The preconditioning was executed according to the requirements from the JESD22-A113F of the JEDEC standard [9]. That is, the samples were first baked at 125°C for 24 hours to remove the moisture inside the packaging structures, and the samples were then soaked at 85°C under 85 % relative humidity (RH) for 168 hours, which is the level 1 of the moisture sensitivity level on JEDEC J-STD-020 standard [10]. Linear current-voltage (I-V) relationships, as the typical I-V curve shows in Figure 3 for the contact resistance measurements, were observed in all of the un-failed samples. After preconditioning, 9/104 (8.65%) and 12/103 (11.7%) of failure rate, respectively for the contact resistance (R_c) of the Kelvin structures and for the total resistance (R_t) of the via-chains, were obtained. In addition, increasing on sample resistance was noted. Table 1 and Table 2 compares the average of sample resistance before and after preconditioning for the testing samples, and it is observed from the table that about 2.59%~4.69% and 0.78%~1.98% of resistance increasing, respectively for R_c and R_t, were obtained. The resistance increasing are believed due to corrosions and thermal induced migrations on the via metals and the interconnection lines.

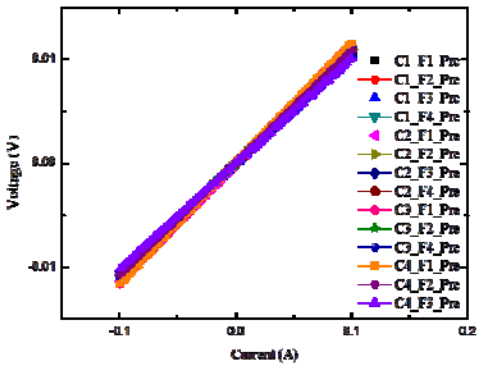

Fig. 3. Typical I-V Curve After Preconditioning.

Table 1: Average Contact Resistance (R_c) for Preconditioning (Unit: mΩ)

Type	Initial	Precondition	Difference

Center	104.87±3.46	109.08±3.85	+4.01 %
Left	109.53±5.22	113.30±6.03	+3.44 %
Right	110.10±4.34	115.26±5.06	+4.69 %
Up	110.57±6.02	114.97±6.64	+3.98 %
Down	112.21±6.24	115.12±6.03	+2.59 %

Table 2: Average Total Resistance (R_t) for Preconditioning (Unit: Ω)

Type	Initial	Precondition	Difference
Center	12.76±0.34	12.93±0.40	+1.33 %
Left	12.82±0.39	12.92±0.39	+0.78 %
Right	12.71±0.47	12.83±0.29	+0.94 %
Up	12.60±0.15	12.70±0.17	+0.79 %
Down	12.65±0.22	12.90±0.62	+1.98 %

IV. THE RELIABILITY TESTS

Based on the sample resistance measured after the preconditioning, reliability tests were next carried out with the temperature cycling tests (TCT) and the temperature humidity cycling tests (THCT). The failure criterion was set as (1) 10% or more on resistance change, or (2) nonlinear I-V curve, or (3) an open circuit, were measured or observed. The tests were executed until 90 cycles or 75% or more samples were failure.

After the experiments, the Weibull distribution function was employed for the reliability analyses. Based on the Weibull distribution, the cumulative distribution function at time *t* is in the form:

$$F(t) = 1 - \exp\left[-\left(\frac{t}{\eta}\right)^{\beta}\right] \quad (1)$$

where η and β are respectively the scale parameter and the shape parameter to be extracted through data fitting. The strength of the fittings was finally checked through the correlation coefficients (ρ).

A. The Temperature Humidity Cycling Test (THCT)

As shows in Figure 4, process of the THCT was modified from the JESD22-A100C standard [11]. That is, the temperature range was set between 30°C and 85°C with 95% relative humidity (RH). Each temperature cycle takes 8 hours with 2 hours for ramp-up and 2 hours for ramp-down, respectively. Totally 91 via-chain samples and 92 Kelvin structure samples after preconditioning were performed for THCT, and resistances of the samples were recorded every 10 cycles.

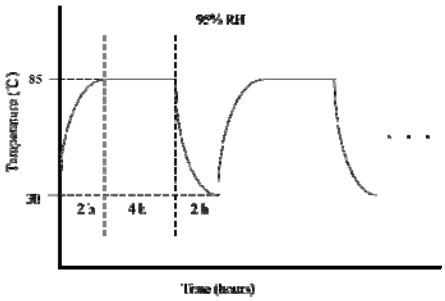

Fig. 4. The THCT process.

The plots in Figure 5 indicate the resistance changes through THCT for several typical Kelvin samples, and similar plots were also obtained for the via-chain samples (not show). It is observed from the figure that the resistance increased dramatically in the first 250 hours (within 30 cycles), and the increments became slow after 500 hours (within 60 cycles). In addition, a drop of resistance change was measured on some Kelvin samples after 550 hours. The researcher defines the number of the failed devices over the total devices number after preconditioning, and demonstrates the relationships between time and cumulative failure rates (shown as Figure 6). It is found that instant failure rates were high at the first 300 hours for both of the testing samples, especially at around 200 hours (within 20 ~ 30 cycles), and then the cumulative failure rates stay at a considerable slow rate after 300 hours. In particular, the cumulative failure rates were found close to saturation after 650 hours.

Furthermore, the Kelvin samples were found weaker than the via-chain samples because the via-chain data were actually the average of the 15 contact resistances plus the 15 resistances from the interconnections.

We next analyzed the Weibull reliability parameters for the samples through the Weibull++ software, version 6. Table 3 listed the extracted Weibull parameters after fitting. Since both of the correlation coefficients in the table

are close to 1, it is concluded that the fitting results are appropriate to extract the parameters and the Weibull reliability model is suitable for the TSV reliability tests.

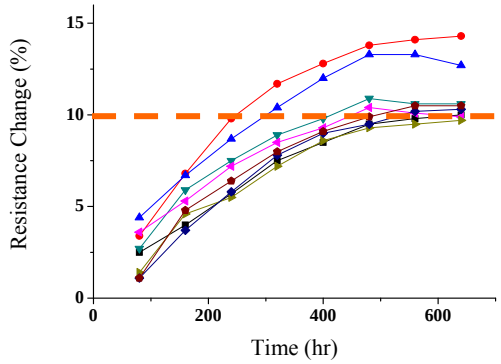

Fig. 5. Resistance changes through THCT for typical Kelvin samples.

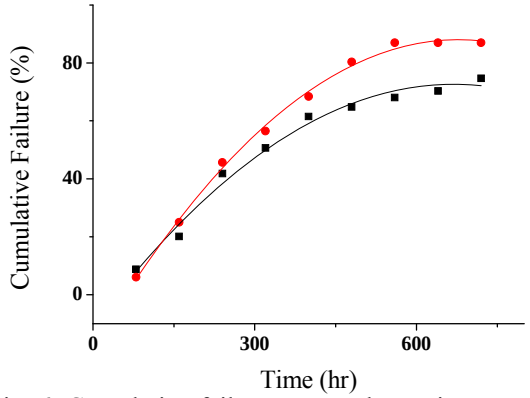

Fig. 6. Cumulative failure rate on the testing samples through THCT.

Table 3: The Weibull Parameters for THCT

Sample Type	Kelvin	Via-Chain
η	379.43	484.18
β	1.603	1.240
ρ	0.986	0.982

B. The Temperature Cycling test (TCT)

The TCT were performed according to JESD22-A104D standard, condition J [12]. That is, the test samples were put into an oven with temperature ranged between 0 °C and 100 °C, and the lower and upper soak time were respectively set 15 minutes (soak mode 4). Due to the limitation of the oven facility, each temperature cycle took 120 min. All of the 50 meander-line samples after preconditioning were used for the TCT in this subsection, and the sample resistances were recorded every 10 cycles.

Figure 7 shows the resistance changes for typical meander samples. The plots indicate that the resistance rises rapidly in the first 80 hours (within 40 cycles), and then increases steadily after 120 hours (within 60 cycles). The plots in Figure 8 describe the time versus the cumulative failure distribution rates for the 50 devices. The data were then analyzed through Weibull++ software, V6. The fitting result for the Weibull parameters are β=2.4499, η=115.06, and ρ=0.980, respectively, and the Weibull reliability model is shown suitable for the TCT tests because the correlation coefficient is close to 1.

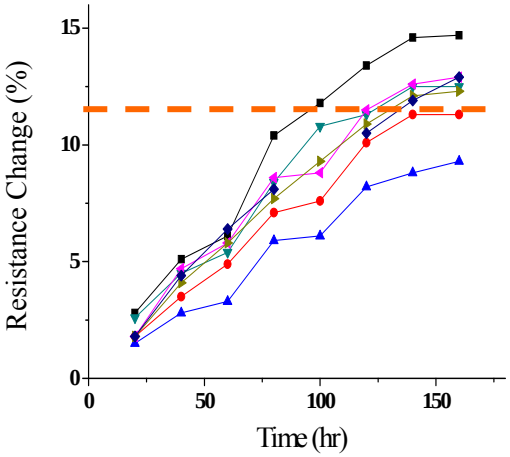

Fig. 7. Resistance changes for typical meander samples through TCT.

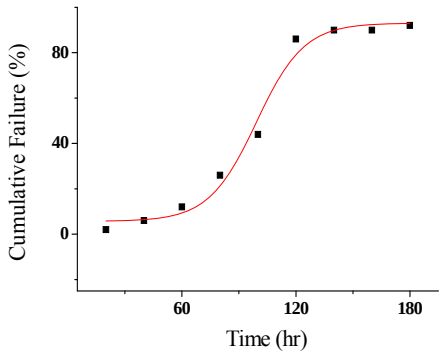

Fig. 8. Time versus failure rate for TCT.

We next traced back the samples to find resistance changes distribution on the test wafer, and the result is shown in Figure 9. In Figure 9, the red and yellow dots respectively represent sample locations with large (over 200%) and medium (50%~200%) resistance change after TCT, and it is found from the figure that the central samples are more robust than the edge samples on a wafer surface.

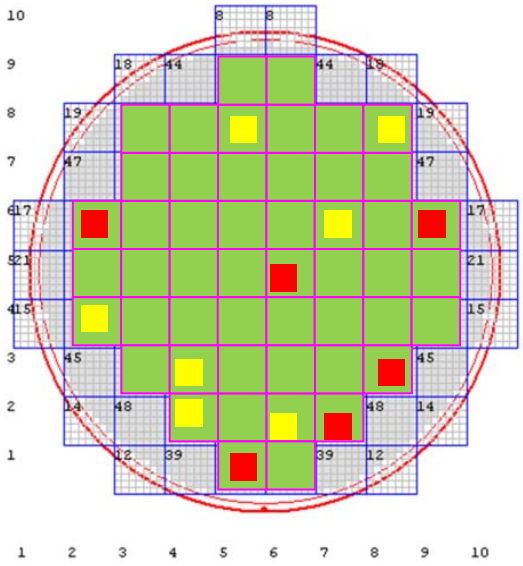

Fig. 9. Distributions of the sample resistance change (red: over 200%; yellow: 50%~200%) after TCT.

C. The Failure Analysis

In order to analyze the failure mode of the samples, we finally performed the cross section observations on TSV through optical microscope (OM) and scanning electron microscope (SEM) with energy dispersive spectrometer (EDS). Figure 10 and 11 respectively shows a typical failed sample from OM and SEM observations, and corrosions and flaking off on metals are noticed. Since metal oxidation and metal de-lamination are also observed for the meander redistribution lines as shown in Figure 12, it is believed that the internal structure stress due to CTE mismatch and moisture permeation accelerate the metal failures.

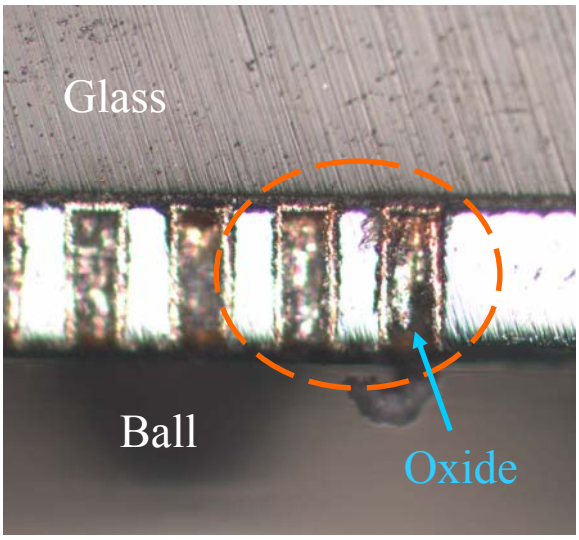

Fig. 10. The sample cross section by OM.

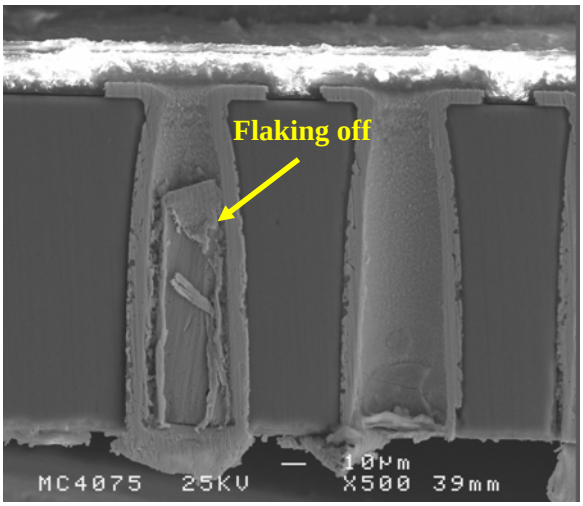

Fig. 11. The sample cross section by SEM with EDS.

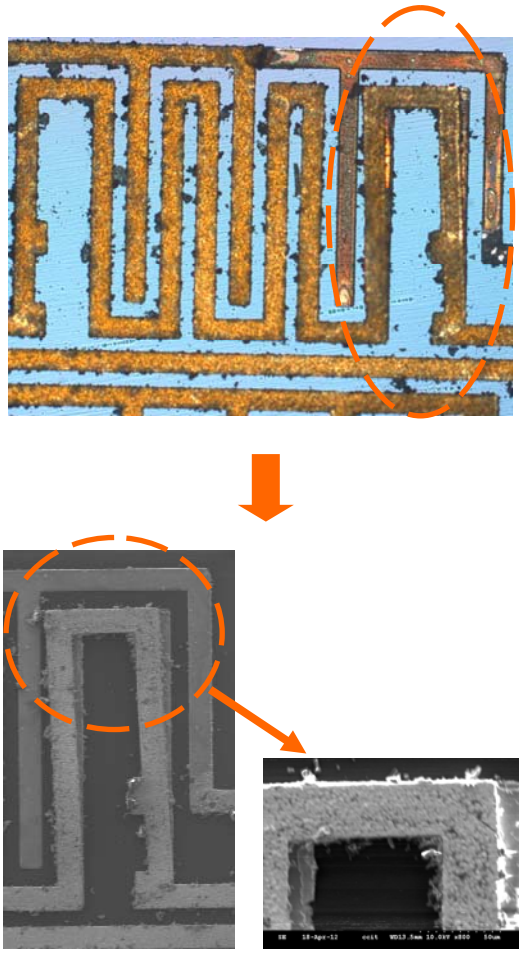

Fig. 12. The meander copper lines by OM and SEM.

V. CONCLUSIONS

In this study, three self-design TSV test patterns were used for reliability tests with enough samples, and resistance of the samples were first found increased due to preconditioning because of the moisture corrosion. Through the temperature cycling tests and the temperature humidity cycling tests after preconditioning, the increasing on sample resistance were recorded and the cumulative failure rate curves were plotted. The Weibull parameters were next extracted through curve fittings from the experimental data, and the values of the extracted coefficient indicate that Weibull reliability model is suitable for TSV reliability tests. Finally, flaking off and de-lamination on metals were observed from failure analyses verifying with OM and SEM with EDS inspections.

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