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Impact of Nitride Process Conditions on SONOS Flash Devices

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ABSTRACT

SONOS (Silicon-Oxide-Nitride-Oxide-silicon) Flash memory has the potential to replace most memory products in the future. However, there are technical problems remain to be solved in the course of developing high-capacity memories. In this work, various process conditions and their influences on device characteristics have been carefully examined and evaluated for possible solution of Gbit solid-state memories. Experimental results indicate that silicon-rich nitride layer has lead to high charge-trapping efficiency and baking process can improve leakage significantly. The research conclusion could provide useful experience and information in process and structure design for Gbit SONOS flash memory applications.

Keywords : SONOS, flash memory, charge-trapping efficiency

氮化矽製程條件對 SONOS 快閃式記憶體元件之影響

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摘 要

SONOS 結構之快閃式記憶體未來有取代大部分記憶產品之潛力；然而在高記憶容量技術的發展過程當中，仍有許多瓶頸尚待克服。本論文中，研究各種不同的製程條件並審慎評估其對元件之影響，期能提供製作十億位元固態記憶體之參考。實驗結果顯示在氮化矽層中提昇矽與氮的相對含量將有效提昇元件的電荷捕捉效率；此外，實驗數據亦指出烘烤效應能明顯的改善漏電流的特性。本研究結論對十億位元 SONOS 快閃式記憶體之製程條件與結構設計當可提供有用之經驗與資訊。

關鍵詞：SONOS，快閃式記憶體，電荷捕捉效率

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I. INTRODUCTION

The rapidly growing market share of memory devices has brought about competitive development of memory technologies. Among various designs, Flash memory has become extremely attractive due to its significant advantages such as non-volatility, repetitive electrical program/erase capability, shock resistance, low power consumption, high endurance, and long retention [1-6]. However, the high-voltage operation requirement and the scaling limit in pushing memory density towards Gbit level have prompted the search of new Flash memory design. In one promising structure, SONOS, the silicon nitride thin film as a replacement of conventional floating gate has been adopted to reduce operation voltage and increase storage density [7-11]. The insulating property of nitride layer has made it possible to scale down the dielectrics further and allows dual-bits-per-cell operation mode [12]. Additionally, SONOS Flash exhibits superior resistance to radiation in contrast to conventional Flash memories [13,14]. In spite of its advantages, there are some reliability issues such as program window decay that need to be resolved before its full-scale replacement of other memory products can be realized. In this work, the influence of nitride process condition such as silicon content ratio control and post-fabrication treatment such as UV exposure and baking on SONOS device performance has been studied.

II. IMPLEMENTATION

The SONOS Flash test devices are fabricated by standard CMOS process on p-type substrate except the ONO structure formation and the key process steps of the dielectrics are described as follow. A 2.8-nm thick tunnel oxide was formed by Low-Pressure Chemical Vapor Deposition (LPCVD) with gas flow ratio of SiH_2Cl_2:N_2O = 10:100 (sccm) at 725℃. Next, a 4.5-nm thick silicon nitride was deposited in a LPCVD reactor under various process conditions. The 4.0-nm thick LPCVD blocking oxide was deposited on top of nitride with same gas flow ratio and temperature as tunnel oxide. The polysilicon deposition and the rest of the process simply followed standard CMOS procedure. For the ease of comparison, both capacitors and transistors have been fabricated and the cross section of the finished SONOS test structure is shown in Fig. 1.

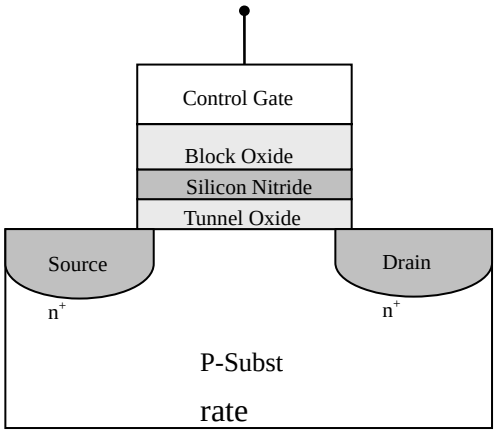


Fig.1. Cross-section view of the SONOS devices.

After the test devices were fabricated, some wafers were illuminated with UV light as standard EEPROM devices would usually be treated and some were also baked for later

comparison. The key processing conditions of the nitride layer and the treatment of finished devices are listed in table I.

Table I. Key process and treatment conditions.

Wafer #	Temp (℃)	SiH_2Cl_2/NH_3 Flow Ratio	UV Exposure	Baked	Si content	wafer name
1	790	1：10			3	1
1	790	1：10		V	3	1B
2	730	1：10	V		2	2UV
2	730	1：10	V	V	2	2UVB
3	730	1：10			2	3
3	730	1：10		V	2	3B
4	730	3：10			1	4
4	730	3：10		V	1	4B

In order to study the influence of various process conditions and treatments on device performance, both DC I-V and high-frequency C-V characteristics have been extracted by a Keithley Semiconductor parameter analyzing system. The electrical characteristics of test devices are mainly utilized to evaluate the leakage and charge-trapping efficiency of SONOS devices.

III. RESULTS AND DISCUSSION

Figure 2 shows the I-V characteristics of SONOS transistors with channel length varies from 0.6m to 10m. It has been verified that Fowler-Nordheim (FN) tunneling mechanism becomes dominant under bias above +10 V and below –7V as demonstrated in the inset of Fig. 2. The smaller slope of the I-V curve within FN-tunnel regime on the left-hand side indicates a lower hole-injection efficiency and hence slower program/erase under negative bias. In addition, channel length has negligible effect on leakage or tunneling characteristics.

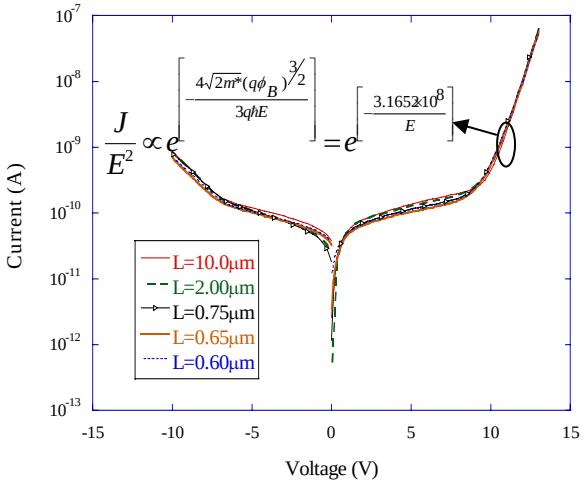


Fig.2. I-V characteristics of transistors with various channel length on test wafer #2.

On the other hand, UV illumination that is used to drive out residual charges in the trapping layer has raised the leakage level by one order of magnitude as shown in Figure 3. The leakage increment may be attributed to the increased defects induced by UV exposure in the tunnel oxide. For further investigation of the influence of UV-illumination on device reliability, the time-dependent leakage behavior of SONOS capacitors (240m × 240m) under constant voltage stress (CVS) has been monitored.

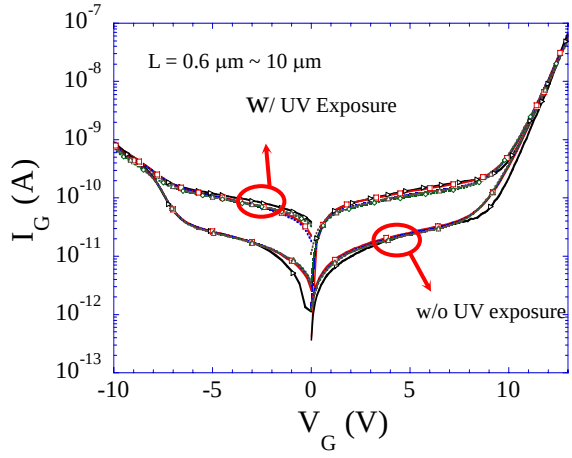


Fig.3. Comparison of I-V characteristics of transistors on test wafer #2 and #3 with and without UV exposure.

Figure 4 shows that the leakage increases significantly after UV exposure. Under positive bias, the initial electron-trapping state even progressively changes into hole-trapping state. This result implies that UV illumination has lead to grown defect (stress-induced hole trapping sites) number in dielectrics and hence oxide degradation that raises leakage level. As a result, data retention time of SONOS devices would be shortened and that is detrimental to long-term data storage. Fortunately, UV exposure-induced leakage can be improved by post-baking treatment.

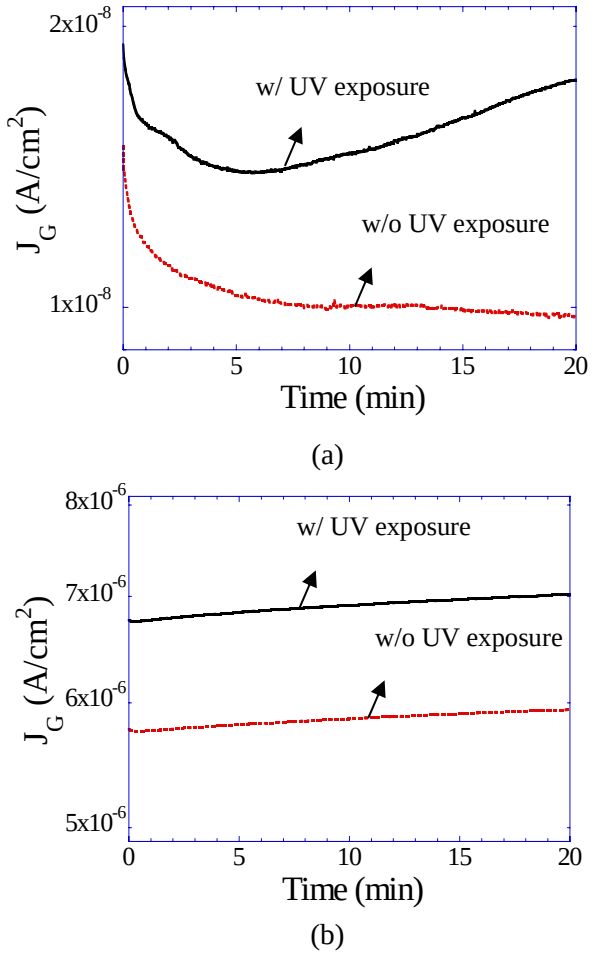


Fig.4. Comparison of J-t characteristics of capacitors on test wafer #2 & #3 under (a) +13 V and (b) –7 V constant voltage stress.

Figure 5 shows that a 250 ℃, 10 hr baking treatment of test devices illuminated by UV light has resulted in a significant leakage reduction. The baking treatment also improves leakage characteristics of the test devices without UV exposure. It is believed that the process-induced defects in the as-deposited dielectrics can be cut down through baking procedure.

For semiconductor memory devices, leakage and charge-trapping efficiency are two major parameters considered in device performance evaluation. Charge-trapping efficiency determines if the memory devices can keep enough charges in the storage nodes after program/erase operation and is reflected in retention characteristics. It is especially critical when the leakage behavior of storage devices is inevitable. For SONOS devices, the nitride layer is responsible for trapping charges and its efficiency in this study is assessed by I-V characterization of transistors and C-V measurement of capacitors.

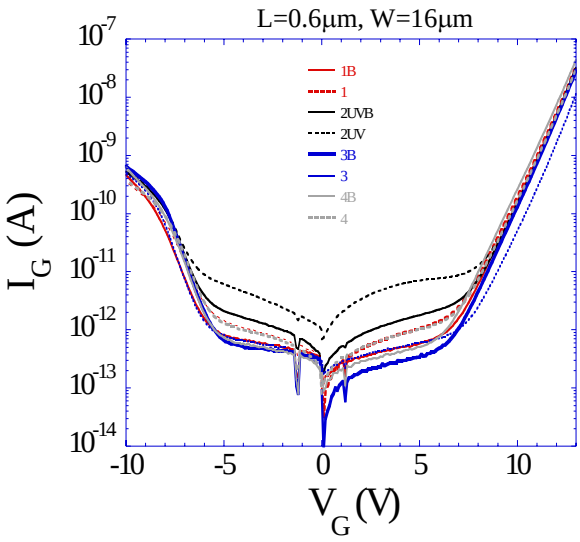


Fig.5. Comparison of I-V characteristics of transistors on all test wafers before with and without baking treatment.

I-V characterization records threshold voltage shift (V_T) of transistors while C-V measurement marks down flatband voltage variation (V_{FB}) of capacitors after program/erase operation. Figures 6 and 7 show the V_T of transistors and V_{FB} of capacitors on UV-illuminated test wafer #2 respectively after program/erase operation. Since V_T and V_{FB} are both proportional to charge-trapping efficiency, they can be used to evaluate the influence of various nitride deposition conditions on SONOS device performance. It is found that under same program/erase operation voltage, V_T and V_{FB} vary if the initial biasing point of reading operation differs. For example, V_T shift towards the left is less if the initial bias is –4 V than that with initial bias of –10 V after –10 V program operation. The variation of V_T and V_{FB} with different initial bias of reading operation can be attributed to the leakage characteristics of SONOS device where a certain amount of charges run off from nitride layer after program/erase.

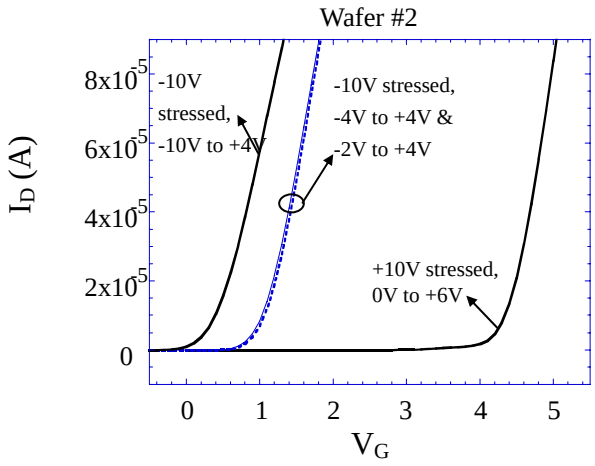


Fig.6. V_T shift of transistors on wafer #2 after program/erase operation by I-V measurement.

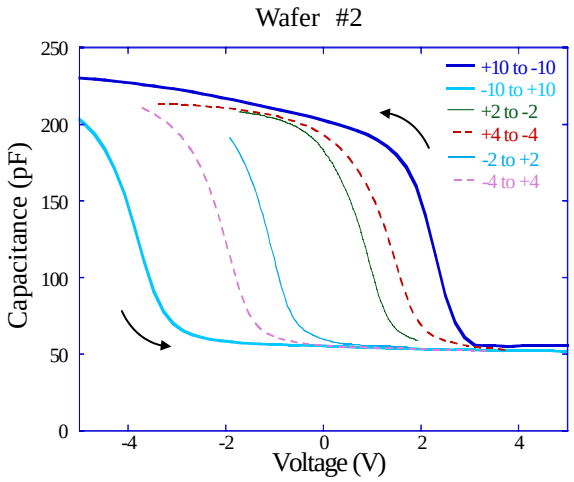
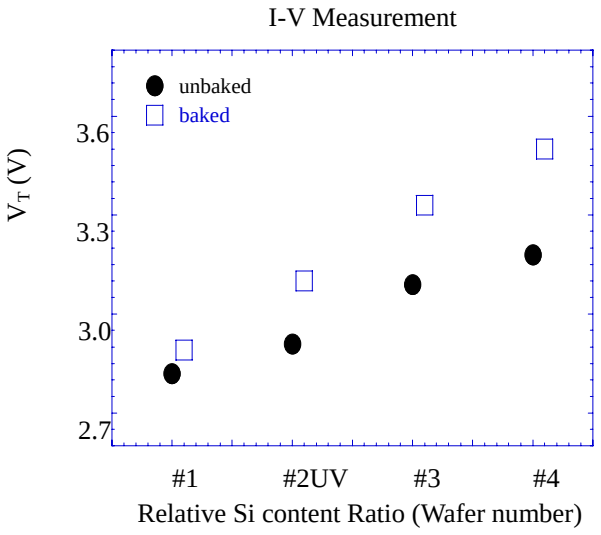


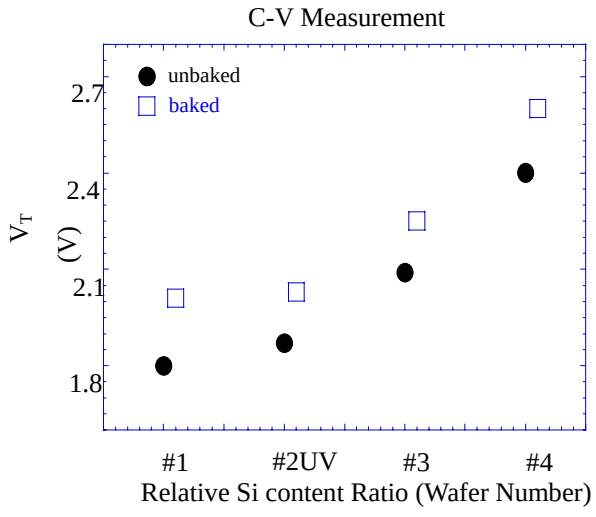
Fig.7. V_{FB} shift of transistors on wafer #2 after program/erase operation by C-V measurement.

Based on V_T and V_{FB} data of all test devices, important trend of processing conditions can be concluded. The relative silicon content in the nitride layer increases with higher SiH_2Cl_2/NH_3 flow ratio or lower temperature [15,16]. Therefore, it can be deduced that the nitride on test wafer #1 contains least silicon content while the nitride on test wafer #4 contains most relative silicon content ratio in table I. The nitride on test wafer #2 and #3 contains same silicon content which is between those on wafer #1 and #4. Experimental data in Fig. 8 show that V_T and V_{FB} increase from wafer #1 to #4 which implies that the charge-trapping efficiency is proportional to relative silicon content ratio in nitride layer. UV exposure has reduced the trapping efficiency while baking treatment has improved the trapping efficiency for all cases. Although silicon content plays an important role in charge-trapping efficiency, it does not have same constructive effect on leakage characteristics. In fact, the leakage level of the

devices on wafer #4 exceeds those on wafer #3. Further study is required to reveal the influence of silicon content on leakage level. The optimum process conditions can be determined based on the analysis procedure described above and they would be very useful in improving SONOS device characteristics.



(a)



(b)

Fig.8. V_T shift of transistors in correspondence with relative silicon content by (a) I-V measurement and (b) C-V measurement.

IV. CONCLUSION

In summary, we have studied various process conditions of nitride layer in SONOS memory devices. It is seen that the relative silicon content has significant influence on device charge-trapping efficiency. A Si-rich nitride film tends to exhibit higher charge-trapping efficiency. However, it might lead to elevated leakage if exposed to UV illumination. Fortunately, baking treatment could amend such flaw. From the above results, silicon-rich nitride with baking treatment has proven to be the most promising candidate for SONOS Flash memory application due to its high charge-trapping efficiency and low leakage..

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